WHAT IS CLAIMED IS:

1. A wafer level testing and bumping process, wherein the wafer has an active surface and at least a fuse line buried inside the wafer, the process comprising the steps of:

forming at least a flip-chip bonding pad and at least a test pad on the active surface such that the test pads are positioned at a peripheral section of the active surface and are electrically connected to the flip-chip bonding pad;

forming at least a fuse window on the active surface such that the upper surface of the fuse window is at a level below the active surface for decreasing the thickness of the structure above the fuse line;

testing the wafer electrically through the test pad to obtain some test results;

determining whether to cut the fuse line by shining a laser beam through the fuse window according to the test results;

forming a patterned passivation layer over the active surface of the wafer, wherein the passivation layer fills the fuse window and covers the test pad but exposes the flip-chip bonding pad; and

attaching a bump to the flip-chip bonding pad.

2. The wafer level testing and bumping process of claim 1, wherein the step of testing the wafer through the test pad furthermore comprises touching the test pad with the tip of a probe pin dangling from a cantilever probe card so that the probe pin is electrically connected to the circuits within the wafer.

3. The wafer level testing and bumping process of claim 1, wherein the wafer furthermore comprises at least a trace line on the active surface such that the test pad is electrically connected to the flip-chip bonding pad through the trace line, and in the step of

forming a patterned passivation layer over the active surface of the wafer, the passivation layer covers the trace line.

4. The wafer level testing and bumping process of claim 1, wherein after the step of attaching a bump to the flip-chip bonding pad, furthermore comprises cutting the wafer up into a plurality of chips.

5. A chip structure with test pads thereon, at least comprising:

a chip with an active surface having at least a flip-chip bonding pad and at least a test pad thereon, wherein the test pad is positioned on the peripheral section of the active surface and is electrically connected to the flip-chip bonding pad; and

a passivation layer formed over the active surface, wherein the passivation layer exposes the flip-chip bonding pad.

6. The chip structure of claim 5, wherein the chip furthermore comprises at least a fuse line buried within the chip and a fuse window having an upper surface below the active surface of the chip for decreasing the thickness of the structure above the fuse line such that the passivation layer fills the fuse window.

7. The chip structure of claim 5, wherein the chip furthermore comprises at least a trace line on the active surface for connecting the test pad to the flip-chip bonding pad and the passivation layer also covers the trace line.

8. The chip structure of claim 5, wherein the chip furthermore comprises a bump attached to the flip-chip bonding pad.